A D-band Frequency-Doubling Solid-State Traveling-Wave Amplifier

Lei Li, Tianze Li, James C. M. Hwang
Department of Material Sci. & Eng.
Cornell University
Ithaca, NY, USA
Email: ll886@cornell.edu

Patrick Fay
Department of Electrical Engineering
University of Notre Dame
Notre Dame, IN, USA
Email: pfay@nd.edu

***Abstract*— We report a solid-state traveling-wave amplifier (TWA) realized through monolithic integration of transistors with a SiC substrate-integrated waveguide (SIW). The TWA uses a stepped-impedance microstrip line as the input divider, but a low-loss, high-power-capacity SIW as the output combiner. The input signal is distributed to four GaN high-electron mobility transistors (HEMTs) evenly in magnitude but with 90° successive phase delays at the fundamental frequency. The HEMTs are distributed in the SIW in a period of a half wavelength at the second harmonic frequency, so that their outputs are combined coherently at the SIW output. To overcome the limited speed of the HEMTs, they are driven nonlinearly to generate second harmonics, and their fundamental outputs are suppressed with the SIW acting as a high-pass filter. The measured characteristics of the TWA agree with that simulated at the small-signal level, but exceeds that simulated at the large-signal level. For example, under an input of 15 dBm at 70 GHz, the output at 140 GHz is 38-dB above that at 70 GHz. Under an input around 70 GHz and 20 dBm, the output around 140 GHz is 14 dBm with a 3-dB bandwidth of 6%. This is not only the first D-band frequency multiplier based on the GaN HEMT technology, but also one with the highest output power and the lowest fundamental leakage among all D-band multipliers of different transistor technologies. This proof-of-principle demonstration opens the path to improve the power, gain and efficiency of sub-terahertz TWAs with higher-performance transistors and drive circuits. Although the demonstration is through monolithic integration, the approach is applicable to heterogeneous integration with the SIW and transistors fabricated on separate chips.**

Keywords*— *frequency multipliers, millimeter wave, MMICs, power combiners, substrate integrated waveguides, traveling wave amplifiers

I. Introduction

With the operating frequencies of next-generation automotive radars and 6G wireless communications extending above 110 GHz, D-band (110–170 GHz) high-power transmitters are needed to over atmospheric attenuation [1]–[3]. However, conventional microwave monolithic integrated circuits (MMICs) based on coplanar or microstrip transmission lines suffer from high loss, significant crosstalk, and limited power capacity above 110 GHz. For example, the output power of D-band MMICs is presently limited to the order of 20 dBm by not only the speed of transistors, but also the loss of power combiners [4]. In particular, the loss of conventional power combiners increases significantly with the number of interconnected transistors, resulting in diminishing return for combining more transistors. By contrast, substrate-integrated waveguides (SIWs) [5] have low loss, minimal crosstalk, and high power capacity. However, because the size of an SIW is on the order of the guided wavelength λ_{SIW} in the SIW, SIWs are usually implemented at the board level as interconnects and transitions [6], filters [7], [8], antennas [9], or power combiners [10] for hybrid integration with transistors.

SIW-based monolithic integration becomes feasible when the frequency exceeds 110 GHz, so that $\lambda_{SIW} \leq 1$ mm in typical semiconductors as Si, GaAs, GaN and SiC. This paper reports monolithic integration of an SIW power combiner with transistors, which can lead to D-band power amplifiers with higher output and efficiency. The SIW-based power amplifier can in turn be monolithically integrated with SIW-based low-noise amplifiers, filters and antennas [11] to realize a single-chip D-band front end. Note that SIW antennas have been monolithically integrated on SiGe transceivers [12], [13].

At the board level, SIW power combiners have been demonstrated in corporate, series, radial, Wilkinson, and Gysel structures [14]. However, these structures when scaled to the D band are too large for monolithic integration. Therefore, we propose a traveling-wave power combiner by embedding transistors in an SIW as illustrated in Fig. 1(a). It can be seen that the propagating wave in the SIW is bounded by two rows of through-substrate vias (TSVs) interconnecting the top and bottom ground planes. Embedded along the middle of the SIW are four "hot" (isolated from the top and bottom ground planes) TSVs separated by $\lambda_{SIW}/2$ from each other. Each hot TSV, when driven by a transistor, can act as an antenna to radiate into the SIW with their radiations coherently combined at the right end of the SIW. The left end of the SIW is shorted by another row of grounded TSVs $\lambda_{SIW}/4$ from the nearest hot TSV, so that the backscattered wave is reflected and added constructively to the forward propagating wave. For a D-band SIW traveling-wave power combiner of 50-μm-thick SiC and Au metallization, Fig. 1(b) shows the HFSS-simulated power-combining loss is 0.7 dB (88% efficiency), which is significantly better than D-band on-chip power combiners based on coplanar or microstrip transmission lines [15]–[17].

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.

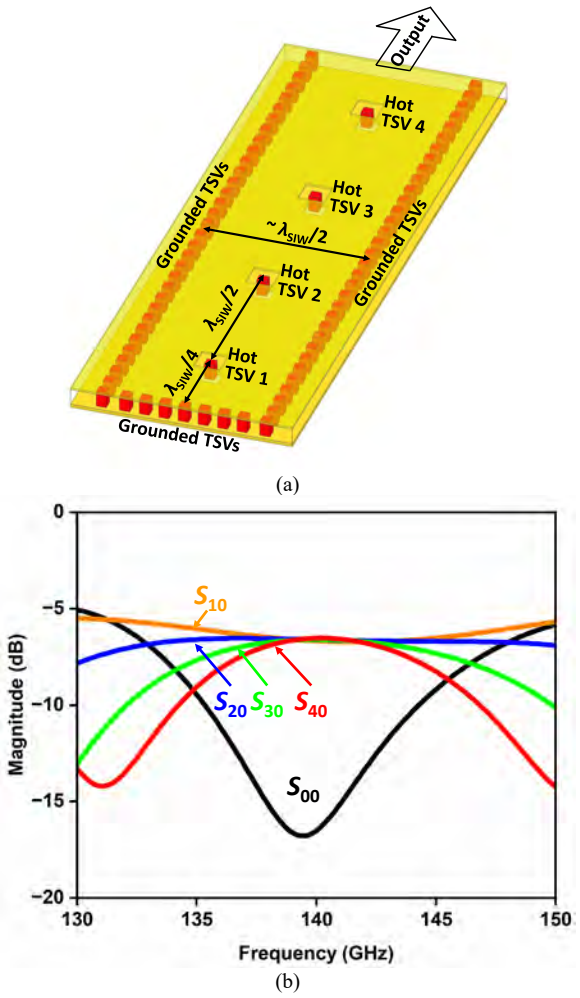


Fig. 1. (a) Schematics and (b) simulated scattering parameters of the proposed SIW power combiner. The four hot TSVs are designated as port 1, 2, 3 and 4, while the output port is designated as port 0.

For high-power GaN-on-SiC MMICs, SIWs are especially attractive because transistors can be monolithically integrated on a SiC SIW without additional process complexity. SiC is an excellent SIW material which offers high dielectric constant for compact size, high electrical resistivity and low loss tangent for low loss, high breakdown strength for high power capacity, strong mechanical toughness for robust fabrication, and high thermal conductivity for heat dissipation [18]. Despite the relatively high power capacity of GaN HEMTs, their speed is limited compared to other transistor technologies. To overcome the speed limit of GaN HEMTs, they can be driven nonlinearly to generate harmonics at higher frequencies. For example, GaN frequency doublers have been demonstrated at 77 GHz with 5-dB conversion loss and 10-dBm output power [19], and at 100 GHz with 4-dB conversion gain and 14-dBm output power [20]. A frequency-multiplying power amplifier can lessen the demand on the transistor cutoff frequency as well as the intermediate frequency.

To demonstrate the novel frequency-doubling power-combining concept, the present traveling-wave amplifier (TWA) is designed with the input divider made of a microstrip

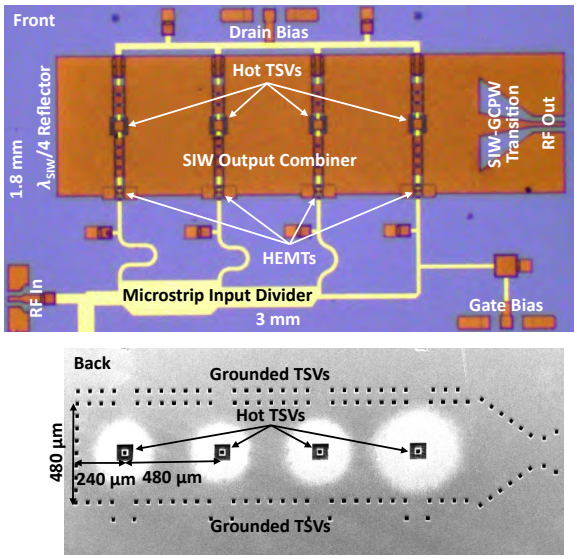


Fig. 2. (top) Front and (bottom) back micrographs of a TWA chip.

line but the output combiner made of an SIW. Besides being low loss with high power capacity, SIW is intrinsically a high-pass filter to suppress the fundamental leakage. The $\lambda_{SIW}/4$ short at the second harmonic frequency on the left end of the SIW also helps suppress odd harmonics. Based on these innovations, we have reported the first D-band frequency doubler based on GaN HEMTs which is also the first SIW-based MMIC power amplifier [21]. This paper expands [21] mainly in design details.

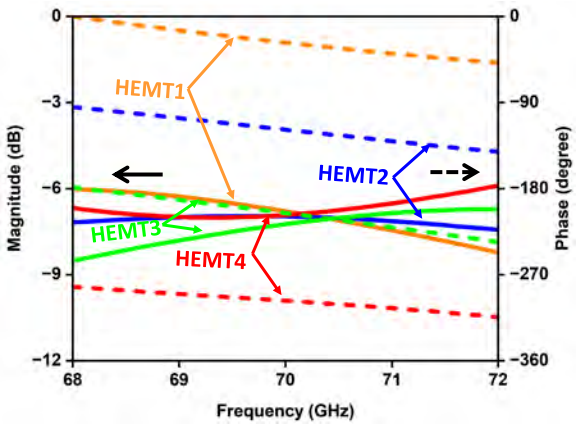
II. Design

The present TWA is designed for fabrication in HRL's T3 40-nm GaN-on-SiC HEMT technology with cutoff frequencies $f_T \sim 200$ GHz and $f_{MAX} \sim 400$ GHz [22]. The SiC substrate is 50-μm thick. Fig. 2 illustrates the 3 mm × 1.8 mm TWA chip. It can be seen that the two TSV rows are 480-μm apart to cut off waves below 100 GHz. In each row, the TSVs have a square cross section of 30 μm × 30 μm and are spaced 60-μm apart center-to-center. The right end of the SIW is transitioned to a grounded coplanar waveguide (GCPW) to facilitate wafer probing [11].

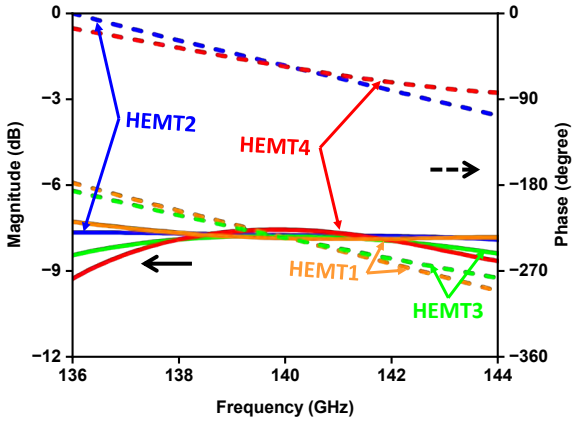
The input signal is distributed through a microstrip line to each HEMT evenly in magnitude but with 90° successive phase delays at the input frequency $f_{IN} = 70$ GHz. Limited to two metal interconnect layers, GCPW lines are laid out in the first metal layer to connect each hot TSV to a HEMT and a common drain bias V_{DD}. The drain bias line is shunted after $\lambda_{GCPW}/4$ by a metal-insulator-metal (MIM) capacitor to prevent RF leakage, where λ_{GCPW} is the wavelength in the GCPW line. Airbridges are designed in the second metal layer to connect the top ground plane of the SIW across the GCPW line. HFSS simulation confirms that the airbridges have little effects on the SIW characteristics.

The input and output impedances of each 2 × 25 μm HEMT are optimized through source- and load-pull simulations using HRL's HEMT model in ADS. Under a class-C gate bias of $V_{GG} = -1$ V, a drain bias of $V_{DD} = 12$ V, and an input power $P_{IN} = 10$ dBm at 70 GHz and $(12 + j80)$ Ω, each HEMT can supply an output power $P_{OUT} = 6.4$ dBm at 140 GHz to a hot TSV with an optimum load impedance $Z_{OPT} = (25 + j60)$ Ω. The load

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.



(a)

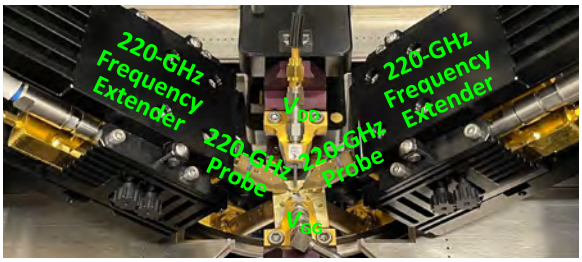


(b)

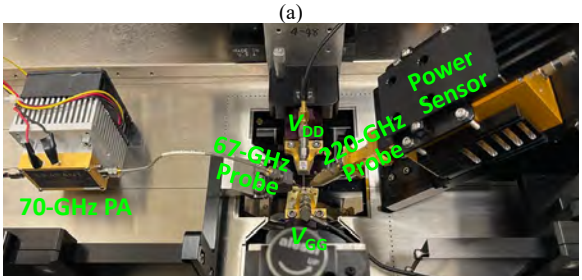
Fig. 3. HFSS-simulated magnitudes and delays (a) from the input of the input divider to the input of each HEMT (dash) and (b) from the output of each HEMT to the output of the output combiner (solid).

impedance presented by each hot TSV is adjusted by tuning its gaps with the top and bottom ground planes, as well as the length (250 μm) and characteristic impedance (22 Ω) of the GCPW line connecting each HEMT to its respective hot TSV. With gaps of 13 μm and 25 μm to the top and bottom ground planes, respectively, a hot TSV has an impedance of $(2.4 - j6.8)$ Ω, which is further transformed to Z_{OPT} through a 22-Ω, 90°-GCPW to Z_{OPT}.

Fig. 2 also illustrates the input divider consisting of a stepped main line and four delay lines branching out from the main line to each HEMT. The input of the divider is designed to match the optimum source impedance while the outputs of the divider provide even magnitudes with successive phase delays to the HEMTs. Broadband phase synchronization between the microstrip divider and the SIW combiner is challenging because quasi-transverse-electromagnetic (TEM) waves travel in the microstrip line whereas transverse-electric (TE) waves travel in the SIW, the latter being more dispersive [23]. Nevertheless, the SIW and the microstrip line can be designed to ensure phase synchronization for both 70-GHz quasi-TEM waves in the microstrip line and 140-GHz TE waves in the SIW as shown in Fig. 3 and detailed below.



(a)



(b)

Fig. 4. (a) Small- and (b) large-signal measurement setups.

The design of the divider starts with the width of the gate feed of each HEMT, which is fixed at 20 μm by the foundry. Therefore, the gate feed is connected to the divider through a 20-μm-wide (characteristic impedance $Z_0 = 72$ Ω). A 150-μm-long line (phase delay $\theta = 33°$) with a 0.75-pF shunt capacitor transforms the input impedance of each HEMT from $12 - j80$ Ω to a real 72 Ω to ease subsequent impedance matching and phase synchronization. For example, different lengths of 72-Ω branch lines before the shunt capacitor can be used to finetune the phase at each HEMT without affecting impedance matching.

As shown in Fig. 2, the main microstrip line has a stepped width (impedance) to broaden its bandwidth and to compensate for its loss, so that the input signal is distributed to the four HEMTs evenly in magnitude. Since the impedance of each branch line presented to the main line is 72 Ω, Z_0 of each stepped section in the main line should be 24, 36, and 72 Ω before branching out to HEMT2, HEMT3, and HEMT4, respectively. After optimization by HFSS, the final width of the main line is stepped from 41 Ω to 24 Ω, 34 Ω, and 66 Ω, respectively. Lower impedances of 34 Ω and 66 Ω rather than 36 Ω and 72 Ω, respectively, are used to compensate for the loss as the input signal travels along the main line. The phase difference at each HEMT is then optimized by the lengths of the 72-Ω branch lines. At the input to the divider, a 70-μm-wide, 150-μm-long series line, together with an 80-μm-wide, 150-μm-long shunt line and a 0.75-pF series capacitor (MIM0) transforms the impedance of the loaded divider to 50 Ω.

III. Measurement

Scattering parameters are measured in a single sweep from 1 to 220 GHz using an Anritsu ME7838G vector network analyzer, with two Anritsu MA25400A frequency extenders and two MPI TITAN T220A-GSG050 probes [Fig. 4(a)] [24]. Tier-1 calibration establishes the reference planes at the probe tips, using the load-reflect-reflect-match method [25], [26] and the MPI TCS-050-100-W impedance standard substrate. Output

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.

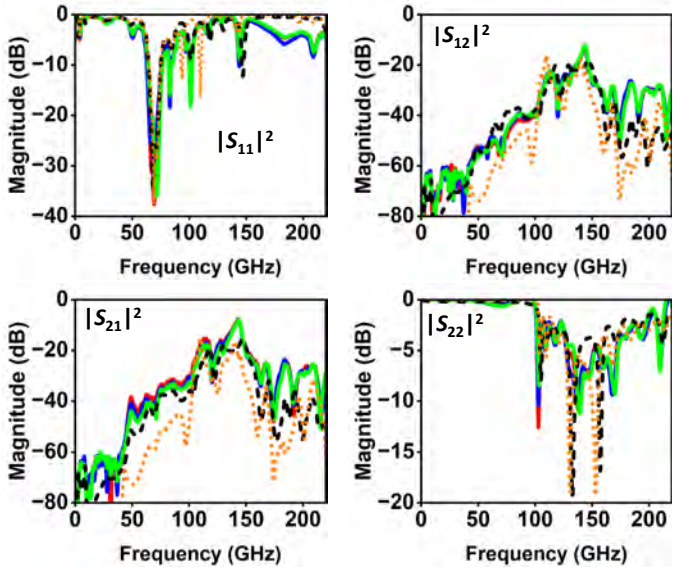


Fig. 5. Measured (solid) vs. HFSS-simulated (dashed) and ADS-simulated (dotted) small-signal characteristics of three TWA chips (red, blue, and green). VGG = −1 V; VDD = 12 V.

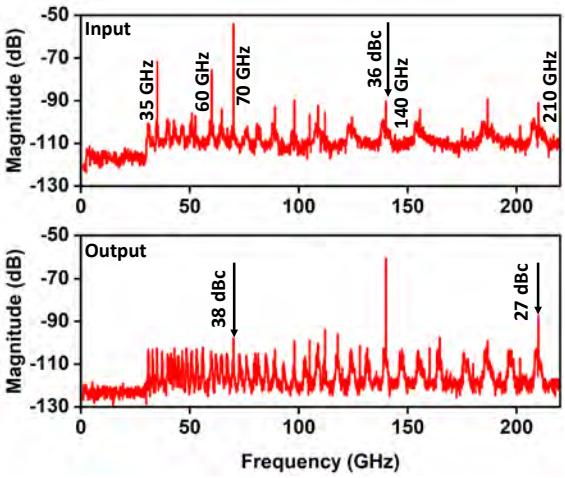


Fig. 6. Measured input and output spectra of a TWA under an input power of 15 dBm at 70 GHz. V_{GG} = −1 V; V_{DD} = 12 V.

spectra are measured from 1 to 220 GHz with the input frequency extender replaced by an Eravant SBP-5037033522-VFVF-S1 50–70-GHz, 22-dBm power amplifier and the input probe replaced by an MPI TITAN T67A-GSG0075 67-GHz probe. A Rohde & Schwarz NRP110T 110-GHz power sensor is used to calibrate the input power through a 150 μm-long coplanar through line with 0.1-dB loss [26]. Output powers are measured around 140 GHz with not only the input reconfigured as for spectrum analysis, but also the output frequency extender replaced by an Erickson PM5B power meter [Fig. 4(b)]. Similar to small-signal measurements, large-signal measurements are calibrated to the probe tips through the low-loss through line. Chips are mounted on a copper carrier hollowed out beneath hot TSVs. Large-signal simulations are performed by using HRL's models up to the seventh harmonic. The simulations use both HFSS and ADS.

IV. Results

Fig. 5 shows that the scattering parameters across the ultrawide bandwidth of 220 GHz of three TWA chips from the same design and wafer. As designed, $|S_{11}|^2$ has a minimum around 70 GHz, $|S_{21}|^2$ and $|S_{12}|^2$ both peak around 140 GHz, and $|S_{22}|^2 > -1$ dB below 100 GHz. It can be seen that the measured values agree with each other as well as that simulated by HFSS. The ADS simulation based on the equivalent circuit reasonably mimics the measurement and HFSS simulation. This help to validate HRL's fabrication and modeling techniques, as well as our measurement and simulation techniques.

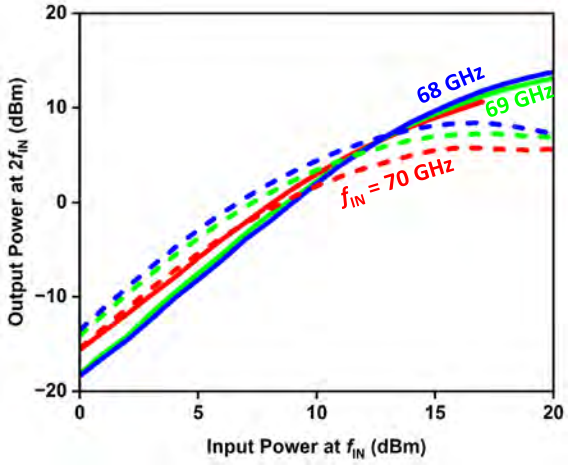
Fig. 6 shows the ultra-wideband 220-GHz input and output spectra of a TWA under P_{IN} = 15 dBm. From the input spectrum, it can be seen that the 140-GHz harmonic is 36 dB below the 70-GHz input signal, indicating the input signal do not have significant harmonic content and the driver amplifier is linear. (We believe the spurious modes at 35 and 60 GHz are from band-stitching issues in the receiver itself rather than the signal source or driver amplifier.) The ratio is reversed in the output spectrum, so that the 140-GHz P_{OUT} is 38-dB higher than the 70-GHz P_{IN}, validating the frequency doubler. The third harmonic of 210 GHz is 27 dB below that at 140 GHz. The noise floor of the output spectrum is approximately 10 dB lower than that of the input spectrum, probably because the SIW power combiner also suppresses the noise below 100 GHz.

Fig. 7(a) shows the power-sweep characteristics of a TWA with f_{IN} as a parameter. Although the Erickson PM5B power sensor is broadband, its measured power of the TWA output is mainly due to the second harmonic around 140 GHz, because the fundamental and third harmonics are < −30 dB below the second harmonic. The WR6 waveguide connecting the TWA to the power sensor also cuts off signals below 110 GHz. It can be seen that P_{OUT} tends to saturate around 14 dBm. For example, under P_{IN} = 20 dBm at 68 GHz, P_{OUT} = 14 dBm at 136 GHz with a DC power consumption of 882 mW. This P_{OUT} at 136 GHz is comparable to that of [20] at 100 GHz, but significantly higher than that of [19] at 77 GHz. Unlike the small-signal model, HRL's large-signal model does not seem to fully capture harmonic generation under gain compression. In the future, the large-signal model can be improved by using our newly established ultra-wideband capability for large-signal characterization of a 70-GHz transistor up to its third harmonics in a single sweep of frequencies. Fig. 7(b) illustrates the bandwidth of the TWA. It can be seen that with P_{IN} = 18 dBm, P_{OUT} > 10 dBm from 132 to 140 GHz, corresponding to a 3-dB bandwidth of 6%. Near the band center, the conversion loss is 5–6 dB.

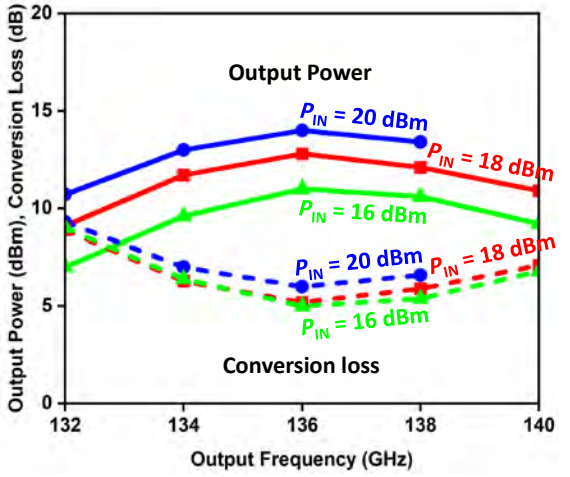
V. Disscussion

TABLE I compares the present D-band frequency multiplier with those reported for different transistor technologies [28]–[47]. It can be seen that this work not only is the first D-band frequency multiplier based on the GaN HEMT technology, but also has the highest output power and the lowest fundamental leakage among all D-band frequency multipliers of any transistor technology. This shows the power of the GaN technology and the benefit of the high-pass of the SIW. Presently the high output power is achieved by combining just four simple 2 × 25 μm HEMTs, whereas most others use

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.



(a)



(b)

Fig. 7. Measured (solid) vs. simulated (dash) output power as a function of (a) input power and (b) output frequency. V_{GG} = −1 V; V_{DD} = 12 V.

multistage driver amplifiers. Therefore, by combining larger transistors and multistage driver amplifiers through the high-power-capacity SIW, higher power, gain, and efficiency can be expected by using the present approach.

VI. Conclusion

At the D band, SIWs are small enough to replace coplanar or microstrip transmission lines in a power combiner for high-power MMICs. For proof of concept, a novel power-combining concept has been demonstrated through monolithic integration of GaN HEMTs with a SiC SIW. With the low-loss and high-power-capacity SIW, much higher output power can be achieved by replacing the present HEMTs with higher-performance transistors and drive circuits. Although the SiC SIW provides an easy entry because of its mechanical strength, the present power-combining concept can be implemented in Si where the SIW is fabricated in an interposer before integration with CMOS chiplets.

TABLE II
D-band Frequency Multipliers

Frequency (GHz)	Tech-nology	Multi-plication	P_{IN} (dBm)	P_{OUT} (dBm)	*GAIN* (dB)	f_{IN} Leak (dBc)	P_{DC} (mW)	Ref.
110–130	GaAs	×2	2	5	3	–25	65	[28]
119–135	InP	×3	3	10	7	–30	45	[29]
134	CMOS	×2	15	4.2	–3.1	NA	790	[30]
138–170	SiGe	×2	3	5.6	4.9	–37	36	[31]
117–129	CMOS	×3×3	10.3	6.3	–2.5	–25	328	[32]
130–154	SiGe	×2×2	8	10	5	–20	610	[33]
120–158	InP	×2	7	4.2	–2	–23	19	[34]
115–147	SiGe	×3×2	4.3	4.5	0.2	–12	310	[35]
129–171	SiGe	×2×2	2	2.2	5	–30	100	[36]
99–132	SiGe	×2×2	3	8.5	12	–30	79	[37]
140–180	InP	×3×2	6.3	4.6	–1.7	–13	100	[38]
108–155	SiGe	×2	0	8.1	13	NA	98	[39]
128–140	SiGe	×2	15	9.4	–1	–20	72	[40]
127–162	FDSOI	×3×2	0	5.1	6.9	NA	47	[41]
110–170	SiGe	×4	5	2.5	11	–29	100	[42]
125–145	FDSOI	×2	11.7	4.1	–5.5	NA	25	[43]
131–145	CMOS	×2×2×2	0	-2.5	–1	–34	41	[44]
137–159	CMOS	×3×2	15.5	-1.2	–0.7	–20	93	[45]
112–125	CMOS	×2	10	7.8	–0.5	NA	88	[46]
118–155	SiGe	×2×2×3	-14	3.5	19	–25	640	[47]
132-140	GaN	×2	20	14	–5	–38	842	This Work

Acknowledgment

This work is supported in part by the US National Science Foundation (NSF) under Grants ECCS-2117305, ECCS-2122323 and ECCS-2132329, the US Army Research Office under Grant W911NF2410023, the US Department of Defense under the State of the Art Radio Frequency Gallium Nitride program, and the Semiconductor Research Corporation and the US Defense Advanced Research Projects Agency through the Joint University Microelectronics Program. This work was performed in part at the Cornell Center for Materials Research which is supported by NSF through Grant DMR-1719875.

References

[1] W. Hong *et al.,* "The role of millimeter-wave technologies in 5G/6G wireless communications," *IEEE J. Microw.,* vol. 1, no. 1, pp. 101–122, Jan. 2021.

[2] C. Waldschmidt, J. Hasch, and W. Menzel, "Automotive radar—From first efforts to future systems, " *IEEE J. Microw.,* vol. 1, no. 1, pp. 135–148, Jan. 2021.

[3] T. Maiwald *et al.,* "A review of integrated systems and components for 6G wireless communication in the D-band," *Proc. IEEE,* vol. 111, no. 3, pp. 220–256, Mar. 2023.

[4] H. Wang et al, "Power amplifiers performance survey 2000-present," [Online]. Available: https://ideas.ethz.ch/Surveys/pa-survey.html.

[5] K. Wu, M. Bozzi, and N. J. G. Fonseca, "Substrate integrated transmission lines: Review and applications, " *IEEE J. Microw.,* vol. 1, no. 1, pp. 345–363, Jan. 2021.

[6] X. Yang *et al.,* "Low-loss heterogeneous integrations with high output power radar applications at W-band," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1563–1577, Jun. 2022.

[7] K. Zhou and K. Wu, "Substrate integrated waveguide multiband bandpass filters and multiplexers: Current status and future outlook," *IEEE J. Microw.,* vol. 3, no. 1, pp. 466–483, Jan. 2023.

[8] B. Yang, Z. Yu, J. Lan, R. Zhang, J. Zhou, and W. Hong, "Digital beamforming-based massive MIMO transceiver for 5G millimeterwave communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3403–3418, Jul. 2018.

[9] H. Saeidi, S. Venkatesh, X. Lu, and K. Sengupta, "THz prism: One-shot simultaneous localization of multiple wireless nodes with leaky-wave

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.

THz antennas and transceivers in CMOS," *IEEE J. Solid-State Circuits*, vol. 56, no. 12, pp. 3840–3854, Dec. 2021.

[10] A. Roev, J. Qureshi, M. Geurts, R. Maaskant, M. K. Matters-Kammerer, and M. Ivashina, "A wideband mm-wave watt-level spatial power-combined power amplifier with 26% PAE in SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.,* vol. 70, no. 10, pp. 4436–4448, Oct. 2022.

[11] M. J. Asadi *et al.,* "Substrate-integrated waveguides for monolithic integrated circuits above 110 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.,* Atlanta, GA, USA, Jun. 2021, pp. 669−672.

[12] X. Yi, C. Wang, X. Chen, J. Wang, J. Grajal, and R. Han, "A 220- to-320-GHz FMCW radar in 65-nm CMOS using a frequency-comb architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 327–339, Feb. 2021.

[13] S. Hu *et al.,* "A SiGe BiCMOS transmitter/receiver chipset with on-chip SIW antennas for terahertz applications," *IEEE J. Solid-State Circuits,* vol. 47, no. 11, pp. 2654–2664, Nov. 2012.

[14] S. H. Shehab, N. C. Karmakar, and J. Walker, "Substrate-integrated-waveguide power dividers: An overview of the current technology," *IEEE Antennas Propag. Mag.,* vol. 62, no. 4, pp. 27−38, Aug. 2020.

[15] X. Li *et al.,* "A high-efficiency 142–182-GHz SiGe BiCMOS power amplifier with broadband slotline-based power combining technique," *IEEE J. Solid-State Circuits,* vol. 57, no. 2, pp. 371–384, Feb. 2022.

[16] S. G. Rao and J. D. Cressler, "A D-band SiGe power amplifier using a four-way coupled-line Wilkinson combiner," *IEEE Microw. Wireless Compon. Lett.,* vol. 31, no. 11, pp. 1239-1242, Nov. 2021.

[17] A. S. H. Ahmed, M. Seo, A. A. Farid, M. Urteaga, J. F. Buckwalter, and M. J. W. Rodwell, "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.,* Los Angeles, CA, USA, Aug. 2020, pp. 492−495.

[18] G. L. Harris, *Properties of Silicon Carbide,* London, UK: INSPEC, 1995.

[19] I. Kallfass *et al.,* "A single-chip 77 GHz heterodyne receiver MMIC in 100 nm AlGaN/GaN HEMT technology," in *IEEE MTT-S Int. Microw. Symp.,* Baltimore, MD, USA, Jun. 2011, pp. 1–4.

[20] T. Sonnenberg, S. Verploegh, M. Pinto, and Z. Popović, "W-band GaN HEMT frequency multipliers," *IEEE Trans. Microw. Theory Techn.,* vol. 71, no. 10, pp. 4327–4336, Oct. 2023.

[21] L. Li, T. Li, P. Fay, and J. C. M. Hwang, "A D-band frequency-doubling distributed amplifier through monolithic integration of SiC SIW and GaN HEMTs," in *Asia-Pacific Microw. Conf. (APMC),* Taipei, Taiwan, Dec. 2023, pp. 1–3.

[22] K. Shinohara *et al.,* "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices,* vol. 60, no. 10, pp. 2982–2996, Oct. 2013.

[23] D. M. Pozar, *Microwave Engineering,* 4th ed, New York, NY, USA: Wiley, 2011.

[24] L. Li *et al.*,, "Single-sweep vs. banded characterizations of a D-band ultra-low-loss SiC substrate integrated waveguide," in *99th ARFTG Microw. Meas. Conf.,* Denver, CO, USA, Jun. 2022, pp. 1–4.

[25] A. Davidson, K. Jones, and E. Strid, "LRM and LRRM calibrations with automatic determination of load inductance," in 36th *ARFTG Conf. Dig.,* Monterrey, CA, USA, Nov. 1990, pp. 57–63.

[26] T. Li, L. Li, and J. C. M. Hwang,"Validity of room-temperature calibration for on-wafer measurements up to 220 GHz, 125 °C, and 48 h," in *ARFTG Microw. Conf.,* San Diego, CA, USA, Jun. 2023, pp. 1–4.

[27] R. B. Marks, "A multiline method of network analyzer calibration," *IEEE Trans. Microw. Theory Techn.*, vol. 39, no. 7, pp. 1205–1215, Jul. 1991.

[28] M. Abbasi et al., "Single-chip frequency multiplier chains for millimeter-wave signal generation," *IEEE Trans. Microw. Theory Techn.,* vol. 57, no. 12, pp. 3134–3142, Dec. 2009.

[29] M. Bao, R. Kozhuharov, and H. Zirath, "A high power-efficiency D-band frequency tripler MMIC with gain up to 7 dB," *IEEE Microw. Wireless Compon. Lett.,* vol. 24, no. 2, pp. 123−125, Feb. 2014.

[30] J. Sharma, T. Dinc, and H. Krishnaswamy, "A 134 GHz +4 dBm frequency doubler at f_{max} in 130 nm CMOS," *IEEE Microw. Wireless Compon. Lett.,* vol. 24, no. 11, pp. 784−786, Nov. 2014.

[31] C. Coen, S. Zeinolabedinzadeh, M. Kaynak, B. Tillack, and J. D. Cressler, "A highly-efficient 138–170 GHz SiGe HBT frequency doubler for power-constrained applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC),* San Francisco, CA, USA, May 2016, pp. 23–26.

[32] B. Khamaisi and E. Socher, "Ku-band to F-band active multiplier chain in 65-nm CMOS," in *Proc. 11th Eur. Microw. Integr. Circuits Conf. (EuMIC),* London, UK, Oct. 2016, pp. 93–96.

[33] A. Bossuet *et al.,* "A 10 dBm output power D-band power source with 5 dB conversion gain in BiCMOS 55 nm," *IEEE Microw. Wireless Compon. Lett.,* vol. 26, no. 11, pp. 930–932, Nov. 2016.

[34] S. Carpenter, Z. S. He, and H. Zirath, "Balanced active frequency multipliers in d and g bands using 250nm InP DHBT technology," in *IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS),* Miami, FL, USA, Oct. 2017, pp. 1–4.

[35] M. Bao, Z. He, T. NgocThi Do, and H. Zirath, "A 110-to-147 GHz frequency sixtupler in a 130 nm SiGe BICMOS technology," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC),* Madrid, Spain, Sep. 2018, pp. 105−108.

[36] M. Kucharski, M. H. Eissa, A. Malignaggi, D. Wang, H. J. Ng, and D. Kissinger, "D-band frequency quadruplers in BiCMOS technology," *IEEE Solid-State Circuits Lett.,* vol. 53, pp. 2465–2478, Sep. 2018.

[37] K. Wu, M. W. Mansha, and M. Hella, "A 99–132 GHz frequency quadrupler with 8.5 dBm peak output power and 8.8% DC-to-RF efficiency in 130 nm BiCMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.,* Los Angeles, CA, Aug. 2020, pp. 476−479.

[38] M. Bao, T. N. Thi Do, D. Kuylenstierna, and H. Zirath, "A 135– 183 GHz frequency sixtupler in 250nm InP HBT," in *IEEE MTT-S Int. Microw. Symp. Dig.,* Los Angeles, CA, USA, Aug. 2020, pp. 480−483.

[39] M. M. Pirbazari and A. Mazzanti, "High gain 130-GHz frequency doubler with Colpitts output buffer delivering pout up to 8 dBm with 6% PAE in 55-nm SiGe BiCMOS," *IEEE Solid-State Circuits Lett.,* vol. 4, pp. 36–39, Jan. 2021.

[40] S. G. Rao, M. Frounchi, and J. D. Cressler, "Triaxial balun with inherent harmonic reflection for millimeter-wave frequency doublers," *IEEE Trans. Microw. Theory Techn.,* vol. 69, no. 6, pp. 2822−2831, Jun. 2021.

[41] S. Li, W. Chen, X. Li, and Y. Wang, "A 5.1 dBm 127–162 GHz frequency sextupler with broadband compensated transformer-based baluns in 22 nm FD-SOI CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC),* Denver, CO, USA, Jun. 2022, pp. 315–318.

[42] M. Ali, G. Panic, and D. Kissinger, "A broadband 110 – 170 GHz frequency quadrupler with 29 dBc harmonic rejection in a 130-nm SiGe BiCMOS technology," in *Proc. 17th Eur. Microw. Integr. Circuits Conf. (EuMIC),* Milan, Italy, Sept. 2022, pp. 44–47.

[43] M. Mock, I. K. Aksoyak, and A. C. Ulusoy, "A high-efficiency D-band frequency doubler in 22-nm FDSOI CMOS," in *Proc. 17th Eur. Microw. Integr. Circuits Conf. (EuMIC),* Milan, Italy, Sep. 2022, pp. 272–275.

[44] J. H. Park, D. Y. Yang, K. J. Choi, and B. S. Kim, "D-band × 8 frequency multiplier using complementary differential frequency doubler," *IEEE Microw. Wireless Compon. Lett.,* vol. 33, no. 3, pp. 311−314, Mar. 2023.

[45] D.-J. Shin, U.-G. Choi, and J.-R. Yang, "A compact D-band CMOS frequency sixtupler using a mode analysis of the harmonics," *IEEE Trans. Microw. Theory Techn.,* vol. 71, no. 4, pp. 1501–1508, Apr. 2023.

[46] Z. Yang, K. Ma, F. Meng, and B. Liu, "A 120-GHz class-F frequency doubler with 7.8-dBm P_{OUT} in 55-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 58, no. 8, pp. 2173–2188, Aug. 2023.

[47] J. Romstadt *et al.,* "A 117.5–155-GHz SiGe ×12 frequency multiplier chain with push-push doublers and a Gilbert cell-based tripler," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2430–2440, Sept. 2023.

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited. Approval ID: <XXXX-2024-XXXX>.